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POWER SUPPLY VOLTAGE MONITOR FOR BUILT-IN TEST EQUIPMENT (BITE) APPLICATIONS

HARRY A. WHEELER

AUGUST 1972

ECOM

UNITED STATES ARMY ELECTRONICS COMMAND · FORT MONMOUTH, N J

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This report describes the design of a power supply voltage monitor capable of monitoring multiple dc voltages simultaneously, indicating out-of-tolerance voltages on one single lamp. Design data and temperature testing results are included for a given design, as well as a computer program for obtaining data for the design of any additional system to be monitored.

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POWER SUPPLY VOLTAGE MONITOR FOR BUILT-IN TEST EQUIPMENT (BITE) APPLICATIONS

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ABSTRACT

This report describes the design of a power supply voltage monitor capable of monitoring multiple dc voltages simultaneously, indicating out-of-tolerance voltages on one single lamp. Design data and temperature testing results are included for a given design, as well as a computer program for obtaining data for the design of any additional system to be monitored.

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POWER SUPPLY VOLTAGE MONITOR FOR BUILT-IN-TEST EQUIPMENT (BITE) APPLICATIONS

INTRODUCTION

A major goal in the Army today is the development of Built-In Test Equipment (BITE) for determining the operational readiness of its electronic systems and for reducing the amount of required forward area maintenance. Maintenance Support Positive, the maintenance concept adopted by the Army, calls for the development of BITE to more easily identify and/or isolate equipment malfunctions. The design work covered in this report pertains to such a capability; that of being able to monitor various working voltages developed by an equipment's power supply and indicate a malfunction, should one or more of these voltages fail.

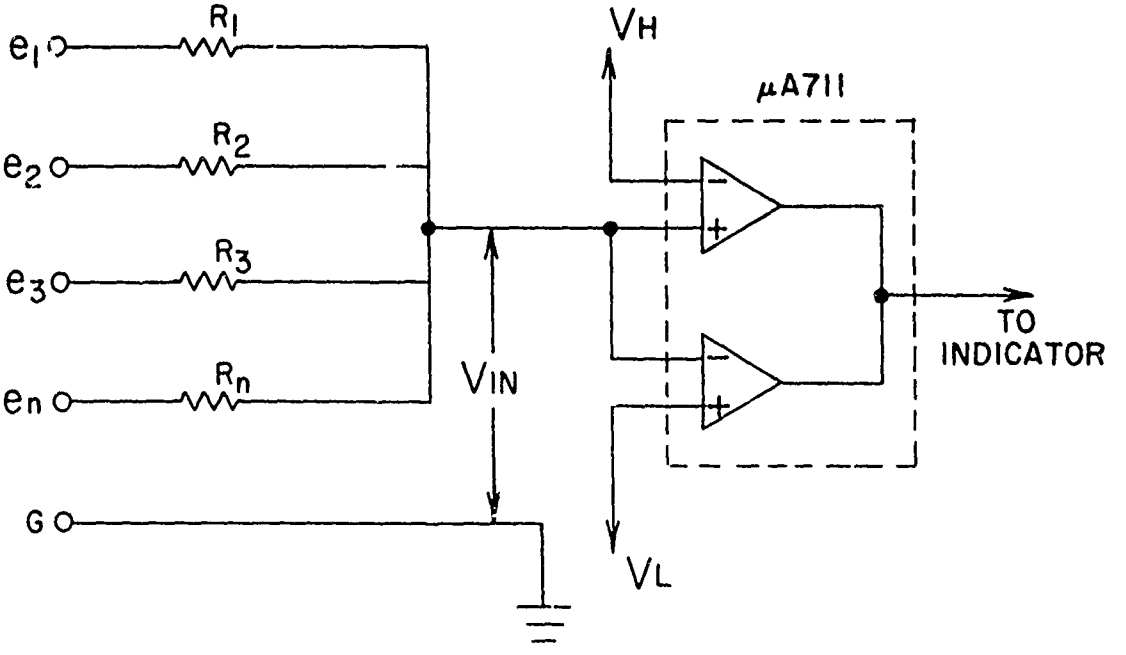
In that the developed circuitry is intended for use in a piece of electronic equipment, its size, weight, cost and power consumption were primary considerations.

This report covers the development effort from the initial design to and through temperature testing. A computer program was also written and a runoff prepared enabling any circuit designer, wishing to monitor supply voltages, to choose the desired voltages and obtain an immediate runoff of the necessary input resistors required to obtain a given set of tolerances.

DISCUSSION

Circuit Design

The basic circuit employed in this design is as follows:



This circuit configuration, using the Fairchild Dual Comparator Type μA711, was selected to facilitate the monitoring of positive and negative voltage variations about a nominal value while still providing a single ended output for the purpose of driving a lamp, meter, or any other type of indicating circuit. Also, since the power supply monitor is intended primarily for BITE applications, the use of a dual comparator in a single package reduces size, weight, wiring complexity, and power consumption compared to the use of two single comparators working in parallel. For example, the use of a μA711 instead of two Fairchild, Type μA710, comparators reduces the power consumption by approximately 50%.

The general operation of the monitor is as follows:

Voltage variations appearing at the input resistors (R_1, R_2, ____, R_n) cause Vin to increase or decrease. This, in turn, causes voltages to appear at the non-inverting and inverting inputs of the comparators. If the voltage variation is positive, it is compared with the upper threshold voltage (V_H) and, if larger, causes a positive voltage to appear at the output of the dual comparator. Likewise, if the voltage variation is negative, it is compared with the lower threshold voltage (V_L) and, if larger, also causes a positive voltage to appear at the output of the dual comparator. In either case, this positive voltage may be used to trigger some sort of indicating device.

A design procedure may be illustrated by going through a specific design application in which three voltages are to be monitored to selected limits with out-of-tolerance conditions indicated on an incandescent lamp. It should be noted that while only three voltages are to be used in this particular example, additional voltages could be monitored if necessary. The schematic shown in Fig. 1 is the resultant circuit and will be referred to throughout the design procedure.

Design Procedure

The specific design application is to monitor the following three voltages to the stated accuracies:

e_1 = +24 volts ±10%

e_2 = +12 volts ±10%

e_3 = +6 volts ±5%

The nominal values for I_1, I_2, I_3, ____, I_n are first selected. These values may be selected at random as long as (I_1) (% tolerance on e_1) =(I_2) (% tolerance on e_2) = ____ = (I_n) (% tolerance on e_n). Also, when using the μA711, I_1 should be greater than 1mA in order to minimize bias current drift. These values determine the relative NO-GO trigger level. In this case, the selected current values were,

I_1 = 1mA, e_1 triggers NO-GO at a 10% variation

I_2 = 1mA, e_2 triggers NO-GO at a 10% variation

I_3 = 2mA, e_3 triggers NO-GO at a 5% variation.

Vin is then chosen at random, but when using the μA711, it must be within the ±5 volt input range of the amplifier (see Fig. 1),

Vin = 0 volts in this case.

Vin is then set to this preselected value by using an input resistor, R_n, connected to a + or - reference voltage (in this case -6V), such that the sum of all input currents = 0 at Vin.

R_1, R_2, _ _ _ _, R_n are then calculated,

$$R_1 = \frac{e_1 - Vin}{I_1} = \frac{24}{.001} = 24K\Omega,$$

$$R_2 = \frac{e_2 - Vin}{I_2} = \frac{12}{.001} = 12K\Omega,$$

$$R_3 = \frac{e_3 - Vin}{I_3} = \frac{6}{.002} = 3K\Omega,$$

and

$$R_n = \frac{e_n - Vin}{-(I_1+I_2+I_3)} = \frac{-6}{-.004} = 1500\Omega$$

V_H, the upper threshold voltage, is then calculated,

$$V_H = Vin + \frac{e_i \times R'_{eq}}{R_i + R'_{eq}}$$

$$= \frac{2.4 \times 923}{24{,}000 + 923} = +0.089 \text{ volts}$$

Where e_i is the change in any individual input voltage necessary to trigger a NO-GO, R_i is the resistance in that leg, and R'_{eq} is the parallel equivalent resistance of all input resistors except R_i.

V_H is the same, as can be expected, regardless of which input branch is selected.

V_L, the lower threshold voltage, is then calculated,

$$V_L = Vin - \frac{e_i \times R'_{eq}}{R_i + R'_{eq}} = -0.089 \text{ volts}$$

The calculation of V_L and V_H assume that the input resistance of the A711 (since operational amplifiers usually have high input resistances) is much greater than the parallel resistance of all the input resistors.

In order to obtain the reference voltages needed for V_H and V_L, simple zener diode networks are used. Referring back to Fig. 1, the impedance looking into each upper and lower limit circuit should be about twice the equivalent resistance of all input resistors in parallel for impedance matching purposes, $R_{eq} = \frac{1}{\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}+\frac{1}{R_m}} = \frac{1}{\frac{1}{24}+\frac{1}{12}+\frac{1}{3}+\frac{1}{1.5}} = 0.89K\Omega$,

$\therefore$ Z (upper and lower limit circuit) $\approx 1.78K\Omega$

Using a IN750 zener diode rated at 4.7 volts,

$$4.7\left(\frac{R_4}{R_4 + R_5}\right) = 0.089 \text{ volts}$$

and

$$\frac{R_4 R_5}{R_4 + R_5} = 1780\Omega,$$

$R_4 = 1814\Omega$ (use $1.8K\Omega$)

$R_5 = 94K\Omega$ (use $90K\Omega$)

i_1 (thru R_4 and R_5) $= \frac{4.7}{95.800} = 49\ \mu A$

i_2 (thru zener) = 8.5 mA (spec)

i_3 (thru R_6) $= i_1 + i_2 \approx 8.5$ mA

$R_6 = \frac{1.3}{.0085} = 153\Omega$ (use 150Ω)

Since $V_L = -V_H$ in this design, the network for V_L is the same as for V_H except that the zener diode polarity is reversed and B^+ is now B^-.

In order to use the output of the μA711 for a lamp indicator, an intermediate transistor switch was required to provide the necessary lamp current. The switch configuration employed is shown in Fig. 1. In designing the switch, the following parameters were used:

β = 100 (2N2222)

V_{BE} = 0.6 volts

I_C = 77.5 mA

Input Voltage = 4.8 volts, therefore,

$\beta I_b = I_c$

$$100 \left(\frac{4.8 - 0.6}{R_7} \right) = 0.0775 \text{ A},$$

$$R_7 \approx 5.4 \text{ K}\Omega \qquad \text{(use 5.6K}\Omega\text{)}$$

Approximating the resistance of the lamp to be 34Ω when hot,

$$\frac{12 - (34 \times 0.0775)}{R_8} = 0.0775 \text{ A},$$

$$R_8 = 120\,\Omega$$

When the monitor circuit was energized and the input voltages set at their nominal values, the lamp remained on. This was found to be a result of the input resistors having ± 5% tolerances. The value of two or more of the resistors deviated from nominal in the same direction and by a magnitude such that their cumulative effects caused an error exceeding that specified for the voltages being monitored. Consequently, the μA711 detected the error and caused the lamp to light.

Since the primary goal at this point was to demonstrate the circuit's plus and minus NO-GO accuracy about a particular voltage, it was decided to compensate for the resistor tolerances by normalizing the nominal value of the voltages being monitored rather than modify the circuit by using precision components or trimming potentiometers. In real applications, trim pots or more accurate resistors could be used to obtain circuit operation at the desired nominal voltages. Consequently, two (2) of the inputs, the 24 volt and 12 volt, were set at their nominal values and the 6 volt input set at 6.7 volts, the optimal setting between the upper and lower NO-GO values. This is seen to be 11.7% above the nominal. The latter percentage was divided by three (3), or 3.9%, and that much was added to the nominal 24 volts and 12 volts and subtracted from the nominal 6.7 volts. The new nominal voltages monitored were then:

$$e_1 = 24.9 \text{ volts} \pm 10\%$$

$$e_2 = 12.45 \text{ volts} \pm 10\%$$

$$e_3 = 6.47 \text{ volts} \pm 5\%$$

Test Results

Data were taken on the subject circuit at room temperature, 0°C, and + 50° C; also, abbreviated tests were made at -4° C and + 70° C.

The data taken at room temperature were more extensive than at 0° C or + 50° C and may be found in Appendix A of this report. In each of three (3) cases, one (1) input voltage was alternately varied while the other two (2) were held constant. As can be seen, the accuracy at room temperature was no worse than 1.3%. Data were also taken, with one (1) input voltage held constant and the other two (2) varying, with equally good results. It was

noted, however, that when one (1) voltage was negative and the other positive (tolerancewise), they added algebraically. It is thus possible to have a voltage variation greater than that desired, when two (2) are off in opposite directions.

In testing the circuit operation at 0° C, one (1) input voltage was alternately varied while the other two (2) were held constant. No error was worse than 1.8%.

Using the same test procedure for operation at $+50^{\circ}$ C, it was determined that the maximum error was 2.63%.

Abbreviated checks were made at $+70^{\circ}$ C and -40° C. The results were slightly worse than at 0° C and $+50^{\circ}$ C; however, no worse than 0.5% over and above the errors at 0° C and $+50^{\circ}$C in any case.

Computer Program

In order to demonstrate the rapid versatility of the design, a program was written and a runoff prepared to facilitate a desired set of voltages and tolerances to be monitored. This demonstrates how easily the input resistors and the threshold voltages may be determined for almost any set of circumstances. The program may be found in Appendix B along with a set of the hypothetical voltages and tolerances to be monitored. The subsequent runoff may then be observed, tabulating all necessary resistances and threshold voltages. It should be noted that the number of voltages to be monitored (N), Vin, the values and tolerances of the monitored voltages (E_i, $\%_i$), and I, must be specified in advance.

CONCLUSIONS

The Power Supply Voltage Monitor described in this report is by no means a panacea, since it does have limitations. First of all, the circuit is subject to algebraic cancellations, due to two (2) or more voltages having tolerances with opposite signs, resulting in a condition where the total voltage variation appears very small even though the individual voltage tolerances may be quite large. Secondly, in order to maintain the nominal voltage values to be monitored at their desired values, cumbersome trim pots or extremely accurate resistors must be employed. This has obvious disadvantages; however, in many real applications, the circuit has a very definite use. In most practical cases, incorrect power supply voltages tend to drift in the same direction precluding the first disadvantage. With a reasonably precise selection of resistors, the second disadvantage may be reduced considerably. All in all, the circuit appears to have many useful applications in BITE and should definitely be considered when prime field equipment is planned in the future. Should a situation arise where three (3) or four (4), for example, voltages are to be monitored very precisely, an individual monitor should be employed for each voltage. A photograph of the Power Supply Voltage Monitor (breadboard) is shown in Figure 2.

BIBLIOGRAPHY

1. James N. Giles, "The μA710 & μA711 High-Speed Comparators," Fairchild Semiconductor Linear Integrated Circuits Applications Handbook, pp. 73-88.

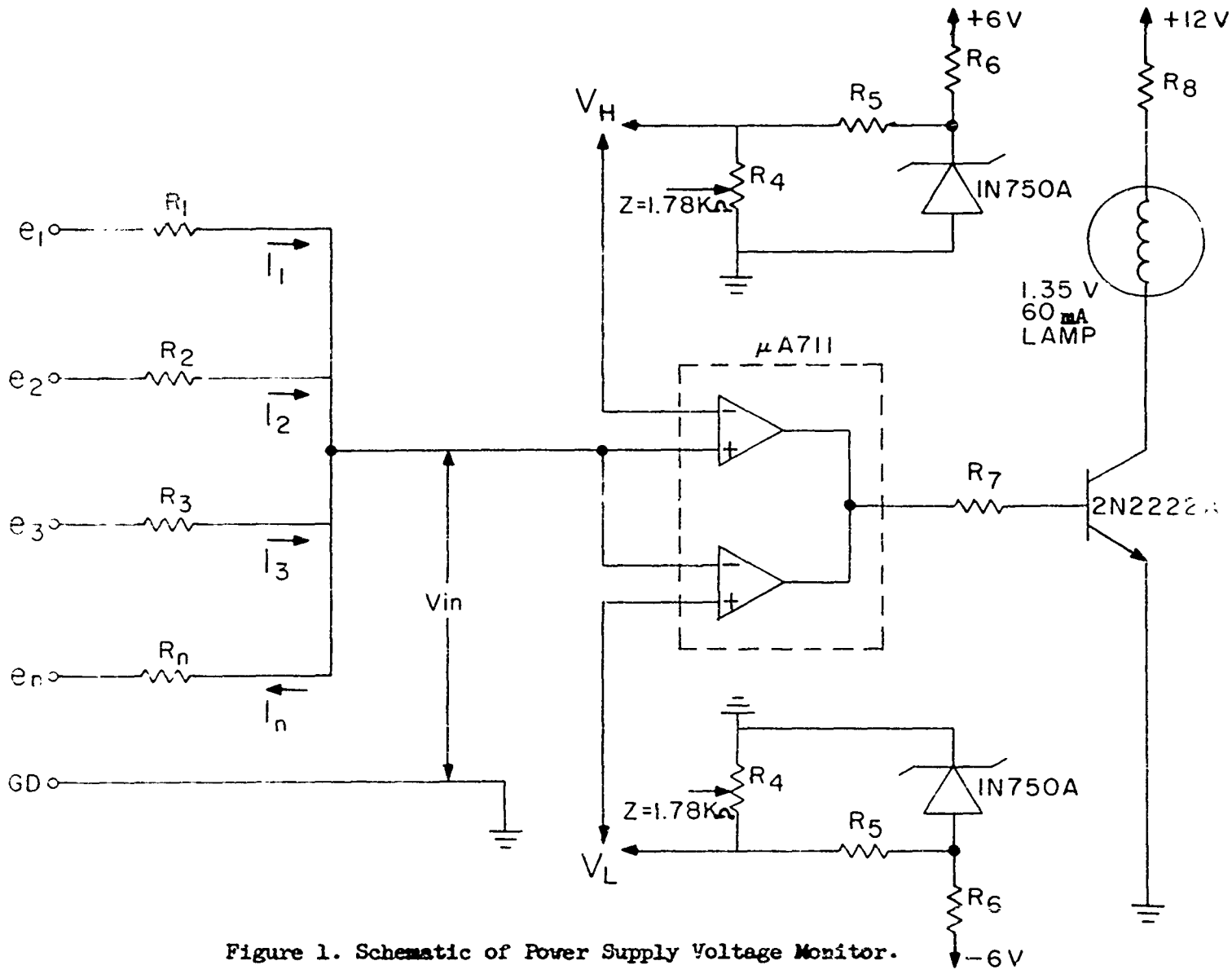


Figure 1. Schematic of Power Supply Voltage Monitor.

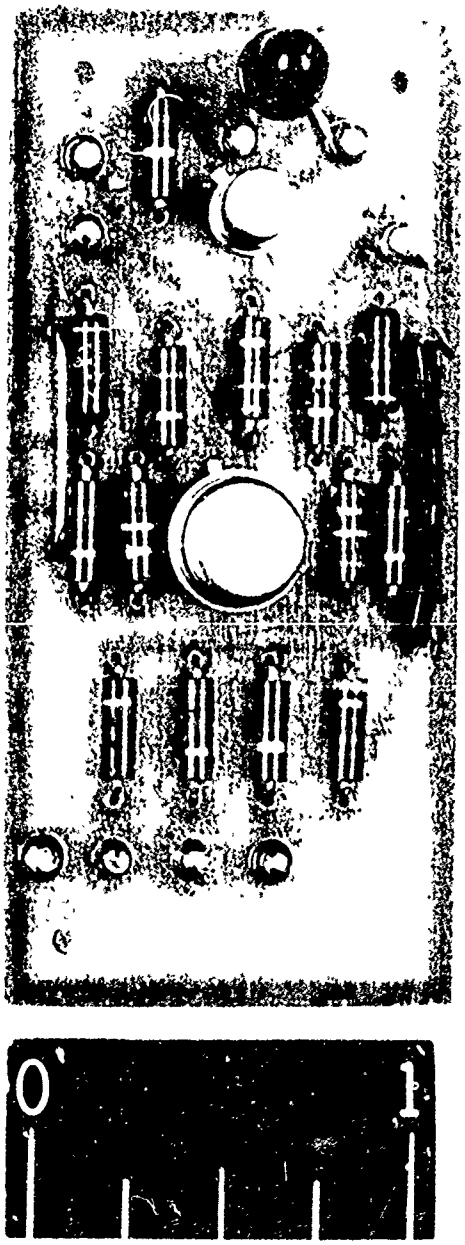


Figure 2. Power Supply Voltage Monitor

APPENDIX A. TEST DATA.

TESTS RUN AT ROOM TEMPERATURE

1. 12V & 6V CONSTANT:

NOMINAL	+10%	−10%	LIGHT ON +	LIGHT ON −	ERROR+	ERROR−	REMARKS
12.45V	-	-	-	-	-	-	-
6.47V	-	-	-	-	-	-	-
24.9 V	27.39V	22.41V	27.75V	22.5 V	0.36V 1.3 %	0.09V 0.4 %	-

2. 24V & 6V CONSTANT:

NOMINAL	+10%	−10%	LIGHT ON +	LIGHT ON −	ERROR+	ERROR−	REMARKS
24.9 V	-	-	-	-	-	-	-
6.47V	-	-	-	-	-	-	-
12.45V	13.7 V	11.2 V	13.75V	11.2 V	0.05V 0.365%	0 V 0 %	-

3. 24V & 12V CONSTANT:

NOMINAL	+5%	−5%	LIGHT ON +	LIGHT ON −	ERROR+	ERROR−	REMARKS
24.9 V	-	-	-	-	-	-	-
12.45V	-	-	-	-	-	-	-
6.47V	6.79V	6.15V	6.8 V	6.16V	0.01V 0.147%	0.01V 0.163%	-

4. 6V CONSTANT & 24V, 12V VARYING ±5%:

NOMINAL	+ 5%	− 5%	LIGHT ON +	LIGHT ON −	ERROR+	ERROR−	REMARKS
24.9 V	26.15 V	23.65 V	-	-	0 0	0 0	Set at ±5% respectively
12.45V	13.07 V	11.83 V	13.1 V	11.75 V	0.03V 0.23%	0.08V 0.676%	-
6.47V	-	-	-	-	-	-	-

5. 12 V CONSTANT and 24 V, 6 V VARYING $\pm$ 5% and $\pm$ 2½%:

NOMINAL	+ 5%	- 5%	+2½%	-2½%	LIGHT ON +	LIGHT ON-	ERROR +		ERROR-		REMARKS
24.9 V	26.15V	23.65V	-	-	-	-	-		-		Set at ± 5%, respectively
12.45V	-	-	-	-	-	-	-		-		-
6.47V	-	-	6.63V	6.31V	6.63V	6.31V	0	0	0	0	-

NOTE: When one (1) voltage is negative and the other positive (tolerance wize), they add algebraically. It is thus possible to have a tolerance greater than that stated when two (2) are off in opposite directions.

TESTS RUN AT 0° C. (Actually -2° to -3° C)

1. 12 V and 6 V CONSTANT:

NOMINAL	+ 10%	- 10%	LIGHT ON +	LIGHT ON-	ERROR +	ERROR -	REMARKS
12.45V	-	-	-	-	-	-	-
6.47V	-	-	-	-	-	-	-
24.9 V	27.39V	22.41V	27.6V	21.6V	0.21V 0.77%	0.19V 0.85%	-

Gradual to full brightness.

2. 24 V and 6 V CONSTANT:

NOMINAL	+ 10%	- 10%	LIGHT ON+	LIGHT ON-	ERROR+	ERROR -	REMARKS
24.9 V	-	-	-	-	-	-	-
6.47V	-	-	-	-	-	-	-
12.45V	13.7V	11.2V	13.6V	11.0V	0.1 V 0.7%	0.2 V 1.8%	-

3. 24 V and 12 V CONSTANT:

NOMINAL	+ 5%	- 5%	LIGHT ON+	LIGHT ON-	ERROR+	ERROR -	REMARKS
24.9 V	-	-	-	-	-	-	-
12.45V	-	-	-	-	-	-	-
6.47V	6.79V	6.15V	6.6V	6.06V	0.01V 0.15%	0.07V 1.14%	-

NOTE: On most readings, the brightness of the light was gradually increasing. The readings, however, were made at maximum brightness.

APPENDIX A (Cont).

TESTS RUN AT +50° C

1. 12 V and 6 V CONSTANT:

NOMINAL	+10%	-10%	LIGHT ON+	LIGHT ON-	ERROR+	ERROR-	REMARKS
12.45V	-	-	-	-	-	-	-
6.47V	-	-	-	-	-	-	-
24.9 V	27.39V	22.41V	28.0V	23.0V	0.61V 2.22%	0.59V 2.63%	-
			↑ GRADUAL	↑ FAST			

2. 24 V and 6 V CONSTANT:

NOMINAL	+10%	-10%	LIGHT ON+	LIGHT ON-	ERROR+	ERROR-	REMARKS
24.9 V	-	-	-	-	-	-	-
6.47V	-	-	-	-	-	-	-
12.45V	13.7V	11.2V	13.8V	11.4V	0.1V 0.73%	0.2V 1.78%	-
			↑ GRADUAL	↑ FAST			

3. 24 V and 12 V CONSTANT:

NOMINAL	+5%	-5%	LIGHT ON+	LIGHT ON-	ERROR+	ERROR-	REMARKS
24.9 V	-	-	-	-	-	-	-
12.45V	-	-	-	-	-	-	-
6.47V	6.79V	6.15V	6.85V	6.17V	0.06V 0.88%	0.02V 0.33%	-
			↑ GRADUAL	↑ FAST			

NOTES

1. Readings made at maximum brightness. If taken at minimum readable brightness, the accuracies would be even better.

2. At +70° C, the results were slightly worse, however, no worse than an additional 0.5% over and above the errors at +50° C in any case.

3. At -40° C, the results were again slightly worse, however, no worse than an additional 0.5% over and above the errors at 0° C in any case.

APPENDIX B. COMPUTER PROGRAM AND RUNOFF.

FILE:POWER -11/02/71 3:53 PM.

```
100 $INCLUDE SETUPR/RNDLIB
200 REAL E(25),PCT(25),I(25),R(25)
300 CALL TIME ON
400 5 WRITE(1,100)
500 READ(1,/)N
600 WRITE(1,110)
700 READ(1,/)VIN
800 WRITE(1,120)
900 DO 10 J=1,N-1
1000 WRITE(1,130)J
1100 10 READ(1,/)E(J),PCT(J)
1200 WRITE(1,140)N
1300 READ(1,/)E(N)
1400 WRITE(1,150)
1500 READ(1,/)I(1)
1600 PCT(N)=0.
1700 DO 20 J=2,N-1
1800 I(J)=I(1)*PCT(1)/PCT(J)
1900 IF (E(J) .EQ. 0.) I(J)=-VIN/ABS(VIN)*I(J)
2000 20 IF (E(J) .NE. 0.) I(J)=E(J)/ABS(E(J))*I(J)
2100 I(N)=0.
2200 DO 30 J=1,N-1
2300 30 I(N)=I(N)-I(J)
2400 DO 40 J=1,N
2500 IF (I(J) .EQ. 0.) R(J)=1.E50
2600 40 IF (I(J) .NE. 0.) R(J)=(E(J)-VIN)/I(J)
2700 SUMR=0.
2800 DO 50 J=2,N
2900 50 SUMR=SUMR+1./R(J)
3000 TERM=E(1)*PCT(1)*.01/(R(1)*SUMR+1.)
3100 VH=VIN+TERM
3200 VL=VIN-TERM
3300 WRITE(1,160)
3400 DO 60 J=1,N
3500 60 WRITE(1,170)J,E(J),PCT(J),I(J),R(J)
3600 WRITE(1,180)VIN,VH,VL
3700 WRITE(1,190)
3800 READ(1,200)A
3900 IF(A .EQ. "YES")GO TO 5
4000 CALL TIME OFF
4100 100 FORMAT(//"N = ")
4200 110 FORMAT("V(IN) = ")
4300 120 FORMAT("ENTER THE VALUES OF ",11H"E" AND "Z")
4400 130 FORMAT(I2)
4500 140 FORMAT("E(",I2,") = ")
4600 150 FORMAT("I(1) = ")
4700 160 FORMAT(////,8X,"E",5X,"PERCENT",5X,"I",8X,"R",/)
4800 170 FORMAT(I2,4(3X,F6.2))
4900 180 FORMAT(//"V(IN) =",F7.3,/"V(H)  =",F7.3,/"V(L)  =",F7.3)
5000 190 FORMAT(//////,"HAVE YOU ANY MORE DATA")
5100 200 FORMAT(A3)
5200 END

 END QUIKLST 1.6 SEC.

 COMPILING.

 END COMPILE 8.3 SEC.
```

NOTE: Wherever F's appear in the text and on this runoff, they are the same as the e's in Fig. 1, printer was only able to print capital F's.

```
TIME ON 1549
 2 NOV 1971



N =
?10←
V(IN) =
?2←
ENTER THE VALUES OF "E" AND "Z"
 1
?6,10←
 2
?-6,10←
 3
?12,15←
 4
?-12,15←
 5
?15,10←
 6
?-15,10←
 7
?18,20←
 8
?24,10←
 9
?5,15←
E(10) =
?-6←
I(1) =
?2←
```

	E	PERCENT	I	R
1	6.00	10.00	2.00	2.00
2	-6.00	10.00	-2.00	4.00
3	12.00	15.00	1.33	7.50
4	-12.00	15.00	-1.33	10.50
5	15.00	10.00	2.00	6.50
6	-15.00	10.00	-2.00	8.50
7	18.00	20.00	1.00	16.00
8	24.00	10.00	2.00	11.00
9	5.00	15.00	1.33	2.25
10	-6.00	0.00	-4.33	1.85

```
V(IN) =  2.000
V(H)  =  2.126
V(L)  =  1.874
```